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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/823,126
Filing Date: March 30, 2001
Appellant(s): FANNING ET AL.

Thinh V. Nguyen
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 2, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-5 and 11-15 (Group 1) and claims 6-10 and 16-30 (Group 2) do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

6,134,633	JACOBS	10-2000
5,996,061	LOPEZ-AGUADO et al.	11-1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-5 and 11-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Lopez-Aguado et al., U.S. Patent 5,996,061.

As to claims 1 and 11, Lopez-Aguado discloses *an apparatus and method* (see Abstract, Figs. 4 and 5) *comprising:*

storage circuit (150) *coupled to a prefetcher* (202) *to store a plurality of prefetch addresses, the plurality of prefetch addresses corresponding to most recent access requests from a processor* (corresponding because most recent access requests that hit in the prefetch cache 106 cause new prefetch addresses to be generated and stored, or more generally simply because the cache and prefetch cache by design store most recently accessed programs and data, and any prefetching necessarily corresponds to those programs and data), *the prefetcher generating an access request to a memory when requested by the processor* ("when requested by the processor" by considering the processor to generally comprise all processing elements above 202 in Figure 5, which

includes array 200 plus 110 and 112 of Figure 4; see col. 5 lines 21-31 and 40-44, and column 7 lines 18-24 and 50-59), and

a canceler coupled to the storage circuit and the prefetcher to cancel the access request when it matches to at least P of the stored prefetch addresses, P being a non-zero integer (since at column 7 line 66 to column 8 line 8, "if the derived prefetch address is already stored in the prefetch queue 150, prefetching is terminated and the derived prefetch address is discarded"), *the canceler including a gating circuit to disable the access request to the memory when the access request is canceled* (a gating circuit to cancel the request is disclosed to the extent claimed, since the claimed function of "disabling when canceled" is met by the "discarding when terminating prefetching" of Lopez-Aguado, and thus the claimed function of a gating circuit is met; additionally, to discard a prefetch address based on the determination to terminate because an address is in the prefetch queue, a terminate or discard signal must be sent or not sent (switched) based upon a control signal (a match to an address in the prefetch queue), which is the basic definition of a gating circuit).

As to claims 2 and 12, Lopez-Aguado teaches the storage element is a queue of predetermined size (150).

As to claims 3 and 13, the queue 150 is a plurality of registers shifting the prefetch addresses, as claimed.

As to claims 4 and 14, matching circuit is inherent to determine if "the derived prefetch address is already stored within the prefetch queue 150" (column 7 lines 66-67).

As to claims 5 and 15, cancel generator as recited is disclosed since the derived prefetch address is discarded (column 8 line 1).

Claims 6-10 and 16-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopez-Aguado et al., U.S. Patent 5,996,061, in view of Jacobs, U.S. Patent 6,134,633.

As to claims 6-10 and 16-20, Lopez-Aguado teaches the invention substantially as discussed above with regard to claims 1-5 and 11-15. Lopez-Aguado does not teach the specific limitation that there are a plurality of comparators to compare the prefetch address with the stored addresses, combining the comparison results, or the matching of entries with a CAM. However, in an analogous prefetching circuit Jacobs teaches a fully associative comparison with elements of the prefetch queue (see Figure 2, and column 6 line 64 to column 7 line 10); this teaching fully embodies all the limitations discussed. That is, "fully associative" memory means that an input address is compared with all stored addresses simultaneously, thus requiring a plurality of comparators, combining results in order to have an indication of a match, and by definition is content addressable and thus a CAM. An artisan would have desired to use a fully associative search for the prefetch address because the parallel comparison with all elements in the storage is faster and removes any considerations as to where elements need to be placed. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to include a plurality of comparators, combining comparison results, and/or a CAM, because it was well

known that such a search in a prefetch queue is fast regardless of where elements are in the queue.

As to claims 21-30, the Lopez-Aguado and Jacobs combination teaches the invention substantially as described above with regard to claims 1-20. Lopez-Aguado does not teach that the storage circuit, prefetcher, and canceler are part of a chipset coupled to the processor. As shown in Figures 3 and 4, these items are apparently disclosed as part of the CPU. However, it is first noted that generally neither the combination or separation of functionally equivalent parts is given patentable weight. Even so, Jacobs shows a processor coupled to the equivalent chipset with prefetch resources at Figure 1 and at column 4 lines 53-62. An artisan would have been motivated to use a chipset as recited coupled to the processor instead of the integrated unit taught by Lopez-Aguado, because these parts might be more readily available, or might already be partly implemented in an existing system, thus saving cost and/or time. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the storage circuit, prefetcher, and canceler in a chipset coupled to the processor, because this might save time and cost by using readily available or existing parts.

(11) Response to Argument

It is first noted that Appellants have not disputed the rejection of the first paragraph of claims 1 and 11 describing the storage circuit and prefetcher, nor the rejection applied to claims 21-30 in which the additional limitation of elements being part of a chipset was addressed.

Appellants argue at 1) on pages 7-8 of the brief that proof of inherency of a gating circuit has not been provided, and further contends that the Examiner has not identified the signal to be gated or the output of the gating circuit. First, the claims do not identify signals to be gated or the output of the gating circuit, only that the gate disable the access request when canceled. Second, hereinabove in the rejection the broadest reasonable interpretation of the relevant claim language includes only the functional description since no particular structure of the gating circuit is claimed, and an apparatus claim must be distinguished from the prior art in terms of structure rather than function – see MPEP 2114. The claimed gating circuit only includes the recited structure of being included in the claimed canceler, and additionally the functional limitations "to disable the access request to the memory when the access request is canceled." It is impermissible to read any other particulars of the gating circuit structure from the specification that are not claimed.

However, even if the entirety of the disclosed gating circuit structure were to be read from the specification into the claims, the gating circuit disclosed only disables the access request if it is determined to be canceled, or otherwise allows the access to memory to pass (present specification, page 11, lines 6-11, and shown at 350 in Figure 3, or at 450 of Figure 4). No other detail or structure is described or required to meet this limitation, simply a circuit that gates (allows or disallows the passing of a signal). In Lopez-Aguado the derived prefetch address is allowed to be passed (to the EMC 108, if the derived prefetch addess is not already in the queue, see Lopez-Aguado col. 8 lines 2-5) or not allowed to

pass (it is discarded if it is already stored in the queue, see Lopez-Aguado col. 7 line 66 to col. 8 line 1), in dependence upon whether it matches an address already in the prefetch queue. As previously stated, this equates to gating of the prefetch address, controlled by the match/no-match of a prefetch address input with those in the queue. Although there are various ways circuitry might be implemented to accomplish this, all such implementations require gating (passing or not passing to memory) the prefetch address based upon whether there is a match, and therefore require a gating circuit as claimed.

Appellants argue at 2) on page 8 of the brief that the derived prefetch address of Lopez-Aguado is not the same as the claimed prefetch address. The Examiner disagrees. First, all prefetch addresses that exist (including those of the present invention) must have been derived (or in other words determined, generated, computed, or calculated). How Lopez-Aguado derives the prefetch address is immaterial to the claim language since the claims state nothing about how the prefetch address is determined. Second, in Lopez-Aguado, the term is clearly to specifically identify a prefetch address that has been newly generated that has not yet been entered into the prefetch queue (has not yet been compared to those in the queue to determine whether it should be passed or not passed). Third, Appellants arguments have not pointed out anything in the claim which differentiates the prefetch address in the claim and the derived prefetch address of Lopez-Aguado.

Appellants argue at 3) on pages 8-9 of the brief that Lopez-Aguado does not match most recent prefetch addresses. The argument that Lopez-Aguado

does not disclose the addresses in the queue represent the most recent access requests is not supported by the claims; the claims state the prefetch addresses *correspond* to the most recent access requests, and such correspondence may be simply due to addresses being part of a same program or data group in the cache and prefetch cache at a certain time. As previously stated hereinabove, caches and prefetch caches by design store the programs and data that have been most recently accessed. Notwithstanding, any prefetch addresses in the queue necessarily *represent* most recent accesses, since in general prefetch addresses in the queue represent programs and data that have been most recently accessed (new prefetch addresses are generated in response to prefetch cache hits as described in the rejection above). The argument that determining if the derived prefetch address is already in the queue is not the same as matching to at least P prefetch addresses in the queue is incorrect, since P is expressly claimed as "a non-zero integer", and therefore determining if a derived prefetch address is already in the queue is the same as matching at least P=1 address in the queue.

Appellants argue at B. on pages 9-10 of the brief that there is no motivation to combined Lopez-Aguado and Jacobs. The argument regarding no gating circuit teaching was addressed hereinabove. The argument regarding no plurality of comparators is incorrect; a fully associative memory (as taught by Jacobs) by definition allows placement of an item into any location and simultaneous comparison of an input address to all of the entries, and therefore requires a comparator at every location to determine where an item is. The

argument regarding Jacobs comparing cache access operations instead of current prefetch requests is not correct; the cache access operations described by Jacobs include the prefetch operations (as cited hereinabove, see Jacobs col. 6 line 64 to col. 7 line 10). Therefore, the teaching of plurality of comparators for comparing an incoming address which may be a prefetch address to a queue of prefetch addresses may be applied to the prefetch queue of Lopez-Aguado as stated hereinabove.

Appellants argue at the third to last paragraph at page 11 of the brief, "Examiner failed to present a convincing line of reasoning as to why a combination of Lopez-Aguado, and Jacobs is an obvious application of prefetch canceling based on most recent accesses." Examiner disagrees, as set out hereinabove the prefetch queue 150 of Lopez-Aguado stores addresses corresponding to most recent access requests, and prefetch canceling occurs when an input address matches one of those in the queue.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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August 6, 2004

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